$PtSe_2$ RF MOSFETs and CMOS Integration

CNF Project Number: 2509-16

Principal Investigator(s): James C.M. Hwang

User(s): Kuanchen Xiong, Lei Li

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Primary Source(s) of Research Funding: U.S. Office of Naval Research Grant N00014-14-1-0653, Air Force Office of Scientific Research, National Science Foundation EFRI 2-DARE Grant No. 1433459-EFMA, NSF Cooperative Agreement DMR-1539916

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Primary CNF Tools Used: ABM contact aligner, Autostep i-line stepper, Oxford PlasmaLab 80+ plasma reactor, SC4500 odd-hour evaporator, Oxford atomic layer deposition (ALD)

Abstract:

Few-layer platinum diselenide ($PtSe_2$) is attractive because it has a sizable bandgap, high carrier mobility, air stability, and can be synthesized below 450°C by thermal conversion or molecular beam epitaxy (MBE). In addition, bulk $PtSe_2$ is a semimetal, which can facilitate low-resistance contacts—a challenge for all 2-D devices to date. Taking advantage of these unique properties, we reported CMOS-compatible ultralow-contact-resistance $PtSe_2$ MOSFETs [2]. However, these devices suffer from poor gate modulation due to the relatively thick $PtSe_2$.

To improve gate modulation, we fabricated MOSFETs on trilayer $PtSe_2$ grown by MBE. The MOSFETs are *n*-type with a current on/off ratio of 43 and 1600 at 290 and 80 K, respectively. These results are among the best of transistors based on synthesized $PtSe_2$. Despite the thin $PtSe_2$ layer, doping by contact bias lowers the contact resistance significantly and boosts the current capacity and the on/off current ratio. Temperature-dependent current-voltage characteristics imply a bandgap of approximately 0.2 eV for trilayer $PtSe_2$, which confirms that the semiconductor-semimetal transition of $PtSe_2$ is not as abrupt as originally predicted.

Summary of Research:

Fabrication. The fabrication process is similar to [2] except for the $PtSe_2$ synthesis methods. The detailed structure of a single device is shown in Figure 1(a). After the deposition of Al_2O_3 as the gate dielectric, the chip was cleaned by acetone, isopropyl alcohol, and deionized water, before drying with N_2.

After it was loaded into a DCA Instruments R450 MBE reactor, it was outgassed for 30 min at 130°C, Growth commenced at 200°C under a Pt flux of $9.2 \times 10^{12}/cm^2 \cdot s$ and an Se flux of $1.6 \times 10^{14}/cm^2 \cdot s$. The Pt and Se fluxes are generated by an electron gun and a Knudsen cell, respectively. After growing for 339 s under both Pt and Se fluxes, the $PtSe_2$ was annealed at 400°C for 30 min under the Se flux alone to enhance its crystal quality.

The resulting $PtSe_2$ is approximately three monolayers (2-nm thick) and (001)-oriented with a high degree of in-plane rotational twin formation.

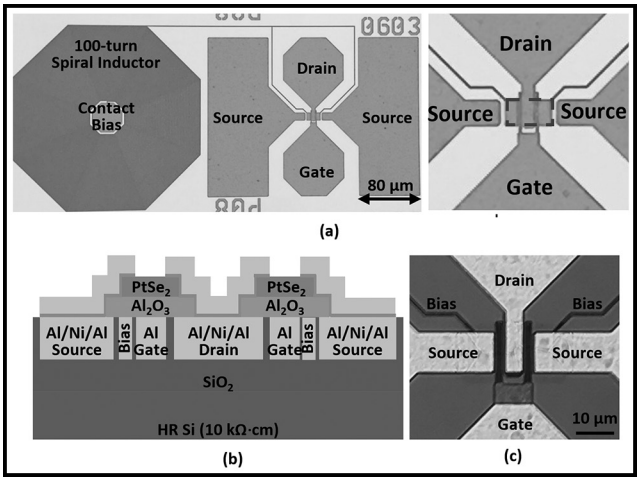

Figure 1: (a) Optical micrograph of individually probable RF MOSFET with source contact biased through a spiral inductor. (b) Cross section schematic. (c) Top-view micrograph of a finished $PtSe_2$ MOSFET.

The trilayer $PtSe_2$ was patterned by photolithography and etched outside the active region by an Oxford PlasmaLab 80+ plasma reactor for 5 s. The flow rates of CF_4 and O_2 were 100 and 20 sccm, respectively. The RF power was 200 W. After $PtSe_2$ etch, the photoresist was stripped by acetone for 30 min. Ni and Al contact layers 50- and 150-nm-thick, respectively, were evaporated by an electron gun.

Figures 1(b) and 1(c) show the cross-section schematic and the top-view micrograph, respectively, of a finished $PtSe_2$ MOSFET.

DC Performance. Figure 2(a) shows the total resistance R_T measured on transfer-length-method (TLM) test structures of different channel lengths. The extraction yields a sheet resistance R_{SH} = 1 × 10^8 Ω/5g and a contact resistance R_C = 2 × 10^8 Ω·μm. Figure 2(b) shows the transfer characteristics of a $PtSe_2$ MOSFET with the drain-source voltage V_{DS} = 3 V and different source contact biases V_{BS}, which helps further reduce the contact resistance as has been demonstrated in [3]. It shows the MOSFET exhibits *n*-type conduction with an on/off ratio of 22. With V_{BS} increasing from 0 to 7.5 V, the on current of the drain I_D^{ON} increases from 60 to 130 nA, while its off current I_D^{OFF} remains the same at 3 nA. Thus, the on/off ratio increases from 22 to 43 mainly due to an increased I_D^{ON}. The results are comparable to $PtSe_2$ grown by chemical vapor deposition.

Thermal Dependence and Bandgap. Figure 3(a) shows the temperature-dependent transfer characteristics of a $PtSe_2$ MOSFET with V_{DS} = 3 V and V_{BS} = 7.5 V. With the ambient temperature decreasing from 290 K to 80 K, the on/off ratio increases from 43 to 1600. This is because I_D^{OFF} decreases much faster than I_D^{ON}, suggesting that they are governed by different activation energies. This difference is confirmed by the Arrhenius plots Figure 3 (b) of the total channel conductance between 80 K and 290 K with V_{DS} = 3 V, V_{BS} = 7.5, and V_{GS} = -5, 0, or 7 V.

The activation energy E_A decreases from 0.18 eV at V_{GS} = -5 V to 0.11 eV at V_{GS} = 7 V. Therefore, the off-state E_A of 0.18 eV should be more indicative of the bandgap of trilayer $PtSe_2$ instead of the on-state E_A.

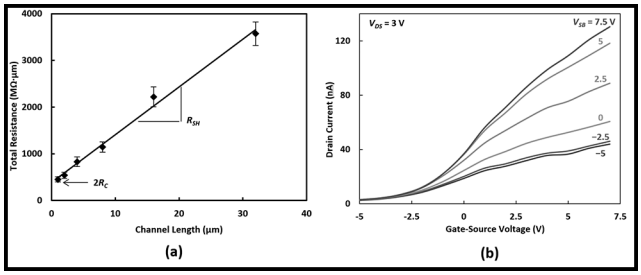

Figure 2: (a) TLM results. (b) Transfer characteristics of a $PtSe_2$ MOSFET under different source contact biases.

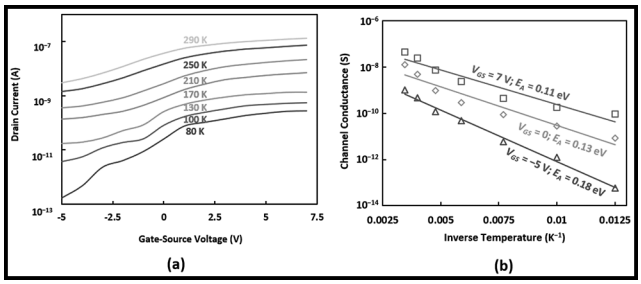

Figure 3: (a) Transfer characteristics of a $PtSe_2$ MOSFET at different temperatures. (b) Channel conductance of a $PtSe_2$ MOSFET between 80 and 290 K.

Future Directions:

First, better MOSFET performance can be expected by growing even thinner $PtSe_2$ uniformly and by thickening the $PtSe_2$ in the contact regions. Second, it is challenging to grow monolayer or bilayer $PtSe_2$ using either MBE or CVD methods. An alternative approach is to use a shadow mask to create the recessed $PtSe_2$ profile.

References:

[1] K. Xiong, et al., "Large-scale fabrication of submicron-gate-length MOSFETs with a trilayer $PtSe_2$ channel grown by molecular beam epitaxy," IEEE Trans. Electron Devices, vol. 67, no. 3, pp. 1-6, March 2020.

[2] L. Li, et al., "Wafer-scale fabrication of recessed-channel $PtSe_2$ MOSFETs with low contact resistance and improve gate control," IEEE Trans. Electron Devices, V65, #10, pp. 4102-08, Oct. 2018.

[3] C. Li, et al., "Black phosphorus high-frequency transistors with local contact bias," ACS Nano, V12, #2, pp. 2118-2125, Jan. 2020.

Fully Transparent FET with High Drain Current and On-Off Ratio

CNF Project Number: 2543-17
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Primary CNF Tools Used: PT720/740, PVD75 sputter deposition, Autostep i-line stepper

Abstract:

We report a fully transparent thin-film transistor utilizing a La-doped $BaSnO_3$ channel layer that provides a drain current of 0.468 mA/μm and an on-off ratio of 1.5×10^8. The La-doped $BaSnO_3$ channel is grown on a 100-150 nm thick unintentionally doped $BaSnO_3$ buffer layer on a (001) MgO substrate by molecular-beam epitaxy. Unpatterned channel layers show mobilities of 127-184 $cm^2V^{-1}s^{-1}$ at carrier concentrations in the low to mid 10^{19} cm^{-3} range. The $BaSnO_3$ is patterned by reactive ion etching under conditions preserving the high mobility and conductivity. Using this patterning method, a sub-micron-scale thin film transistor exhibiting complete depletion at room temperature is achieved.

Summary of Research:

In summary, a fully transparent submicron TFT based on $BaSnO_3$ has been fabricated with a high drain current and on/off current ratio. This breakthrough is made possible by (1) high mobility bare films in combination with (2) the development of a micrometer-scale etching method that preserves the surface roughness, conductivity, and mobility of $BaSnO_3$ films.

These results demonstrate the tremendous potential of $BaSnO_3$ for the future of transparent electronics. The channel is 0.3 μm long and 0.93 μm wide. This is the first demonstration of a submicron scale $BaSnO_3$-based field effect transistor with complete depletion at room temperature. This result has been published in APL Materials January 2020. Two patent applications have been filed on the reactive ion etching of $BaSnO_3$.

References:

[1] J. Park, H. Paik, K. Nomoto, K. Lee, B.-E. Park, B. Grisafe, L.-C. Wang, S. Salahuddin, S. Datta, Y. Kim, D. Jena, H. G. Xing, and D. G. Schlom, APL Mater. 8, 011110 (2020)

[2] H. J. Kim, U. Kim, H. M. Kim, T. H. Kim, H. S. Mun, B.-G. Jeon, K. T. Hong, W.-J. Lee, C. Ju, K. H. Kim, and K. Char, Appl. Phys. Exp. 5, 061102 (2012).

[3] U. Kim, C. Park, T. Ha, Y. M. Kim, N. Kim, C. Ju, J. Park, J. You, J. H. Kim, and K. Char, APL Mater. 3, 036101 (2015).

[4] J. Yue, A. Prakash, M. C. Robbins, S. J. Koester, and B. Jalan, ACS Appl. Mater. Interfaces 10, 21061 (2018).

[5] J. Park, U. Kim, and K. Char, Appl. Phys. Lett. 108, 092106 (2016).

[6] J. Shin, Y. M. Kim, Y. Kim, C. Park, and K. Char, Appl. Phys. Lett. 109, 262102 (2016).

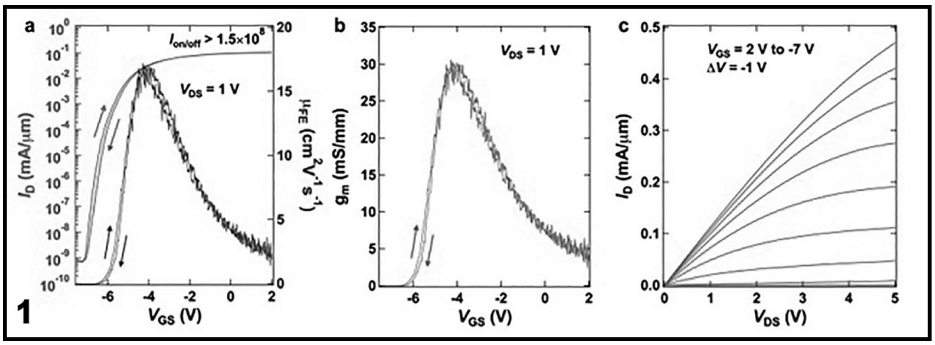
[7] C. Park, U. Kim, C. J. Ju, J. S. Park, Y. M. Kim, and K. Char, Appl. Phys. Lett. 105, 203503 (2014).

[8] Y. M. Kim, C. Park, T. Ha, U. Kim, N. Kim, J. Shin, Y. Kim, J. Yu, J. H. Kim, and K. Char, APL Mater. 5, 016104 (2017).

[9] Y. M. Kim, C. Park, U. Kim, C. Ju, and K. Char, Appl. Phys. Exp. 9, 011201 (2016).

[10] J. Park, U.S. patent application No. 16/706,126, Docket# 1126-051 (filed, December 6 2019).

[11] J. Park, U.S. patent application No. 16/706,126, Docket# 1126-052 (filed, December 6 2019).



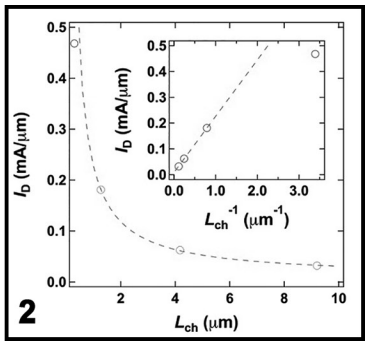


Figure 1, left: (a) The transfer characteristic of the TFT based on La-doped $BaSnO_3$ at V_{DS} = 1 V and the field-effect mobility. The peak field-effect mobility is 17.2 $cm^2V^{-1}s^{-1}$, and the on-off ratio is over 1.5 × 10^8. The subthreshold swing is 0.15 V dec^{-1}. (b) Transconductance of the device at V_{DS} = 1 V. The maximum transconductance is 30.5 mS/mm. (c) The output characteristic of the device at V_{GS} = 2, 1, 0, -1, -2, -3, -4, -5, -6, -7 V. The maximum drain current exceeds 0.467 mA/μm.

Figure 2, right: Drain current dependence on channel length (L_{ch}) when V_{GS} = 2 V and V_{DS} = 5 V. The drain current (I_D) is inversely proportional to the overall channel length except at the shortest channel length, showing little degradation with respect to device scaling. The deviation from linear behavior in the inset at the shortest channel length is likely due to the contact resistance and not short channel effects such as velocity saturation.

Injectable Micro-Scale Opto-Electrically Transduced Electrodes (iMOTEs)

CNF Project Number: 2578-17

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Primary Source(s) of Research Funding: National Institute of Health

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Primary CNF Tools Used: ABM contact aligner, AJA sputter, Westbond 7400A Ultrasonic wire bonder, Oxford 100, Oxford 81, Oxford 82, Unaxis deep Si etcher, Oxford PECVD, Oxford ALD, Anatech, P7 profilometer, ZEISS Ultra and Supra scanning electron microscopes (SEMs)

Abstract:

Recording neural activities in live animals is critical to advancing our understanding of the brain, with far-reaching consequences in healthcare as well as philosophy. Such neural recording can be broadly categorized into two groups — tethered and untethered. An example of tethered neural recording is an electrodes array that can be inserted into the brain, which is then connected to the outside world directly via a wire. Naturally, such a tethered approach is not only inconvenient, but also creates chronic damage due to the residual motion between neurons and electrodes as the brain moves. Hence, there has been much interest in developing tetherless neural recording units.

While RF Coil [1] and ultrasonic approaches [2] have shown promise, the physics of such transduction limits their scaling much below a millimeter. On the other hand, optical techniques, which are becoming increasingly powerful, are nonetheless limited to subsets of neurons in any given organism, impeded by scattering of the excitation light and emitted fluorescence, and limited to low temporal resolution [3].

In this work, we combine the merits of electronics and optics to develop an extremely scaled, untethered electrode unit, where an AlGaAs micro-light emitting diode (μLED) is heterogeneously integrated on top of conventional CMOS. These micro-scale opto-electrically transduced electrodes (MOTEs) are powered by, and communicated through the microscale optical interface (μLED) while the CMOS provides low power amplification and signal encoding. Such MOTEs combine the benefits of optical techniques with high temporal-resolution recording of electrical signals, and are the smallest neural recording units to date (~ 60 μm × 30 μm × 330 μm).

Summary of Research:

Our fabrication starts with a 5 mm × 5 mm, conventional 180 nm CMOS die, which contains the electronics for signal amplification, encoding, and transmission [4]. The CMOS die is then integrated with an aluminum gallium arsenide (AlGaAs) diode, which acts as a photovoltaic (PV) as well as LED, hence abbreviated as PVLED. The PVLED provides an optical link which powers the electronics and transmits encoded signals in optical pulses. The MOTE utilizes Pulse Position Modulation (PPM) for signal encoding for its high information-per-photon efficiency [5], where the spacing between the output pulses is proportional to the measured electric field of neuronal signals across the measurement electrodes. Figure 1 depicts a conceptual deployment of the MOTE [6].

The AlGaAs diodes are first fabricated on a sapphire wafer, to be later released from the sapphire substrate with a sacrificial poly(methyl methacrylate) (PMMA) polymer. In the meantime, the substrate is flattened by Oxford 81 plasma etcher to promote the adhesion between the PVLEDs and the CMOS. Once the PMMA-coated AlGaAs diodes are transferred onto the CMOS die, high vacuum annealing leaves only the PVLEDs array on the CMOS die. To establish the electrical contact between the PVLED and CMOS, we have used ABM contact aligner for photolithography with AZ nLof2020 UV photoresist for efficient lift-off process that ensues after the metal deposition.

After the contact fabrication, the contacts of CMOS and PVLED are connected via similar photolithography process, and to maximize the conformality of the routing metal, we employ the CNF's AJA sputtering system. Following the routing step, each MOTE is etched using Oxford 100 etcher and Unaxis deep reactive ion etch (DRIE) to be separated from the array. Following the etch, each MOTE is encapsulated using Oxford ALD and PECVD for SiO_2, Si_3N_4, and Al_2O_3 deposition.

Finally, the substrate is turned upside down for backside thinning. Figure 2 summarizes the fabrication sequence described herein.

It should be noted that before making much changes are made in fabrication flow, to confirm the functionality of each module (CMOS and the diode), we use the Westbond 7400A Ultrasonic wire bonder for board-level testing. ZEISS Ultra and Supra scanning electron microscopes (SEMs) are also used to inspect the fabricated iMOTE for debugging purposes.

Conclusions and Future Steps:

We have demonstrated that such heterogenous integration fabrication is not only feasible but scalable with high yield (> 80%). The high-quality dielectric deposition tools available at CNF (ALD, PECVD, etc.) allow for excellent cladding that protects the MOTEs in a biological environment (> six months in phosphate buffered saline solution, and > two months in a mouse brain). We plan to continue optimizing the fabrication processes, CMOS circuitries and the PVLED efficiencies so that the MOTEs can be deployed deeper in the brain or to another biological environment. In parallel, we will continue our *in vivo* studies to demonstrate the neural recording based on MOTEs in a mouse brain.

References:

[1] R. R. Harrison, et al., "A Low-Power Integrated Circuit for a Wireless 100-Electrode Neural Recording System," in IEEE J. Solid-State Circuits, vol. 42, no.1, pp. 123-133, Jan. 2007.

[2] D. Seo, et al., "Neural Dust: An Ultrasonic, Low Power Solution for Chronic Brain-Machine Interfaces," arXiv:1307.2196, 2013.

[3] W. Yang and R. Yuste, "*In vivo* imaging of neural activity," Nature Methods, vol. 14, no. 4, pp. 349-359, April 2017.

[4] S. Lee, et al., "A 250 μm × 57 μm Microscale Opto-electronically Transduced Electrodes (MOTEs) for Neural Recording," IEEE Transactions on Biomedical Circuits and Systems, vol. 12, no. 6, pp. 1256-1266, December 2018.

[5] H. Hemmati, et al., "Deep-Space Optical Communications: Future Perspectives and Applications," Proceedings of the IEEE, vol. 99, no. 11, pp. 2020-2039, August 2011.

[6] S. Lee, et al., "Fabrication of Injectable Micro-Scale Opto-Electronically Transduced Electrodes (MOTEs) for Physiological Monitoring," IEEE Journal of Microelectromechanical Systems, submitted.

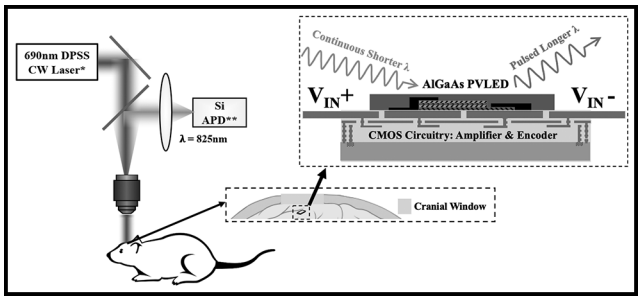

Figure 1: An envisioned employment of the MOTE for neural recording (see ref. [6]).

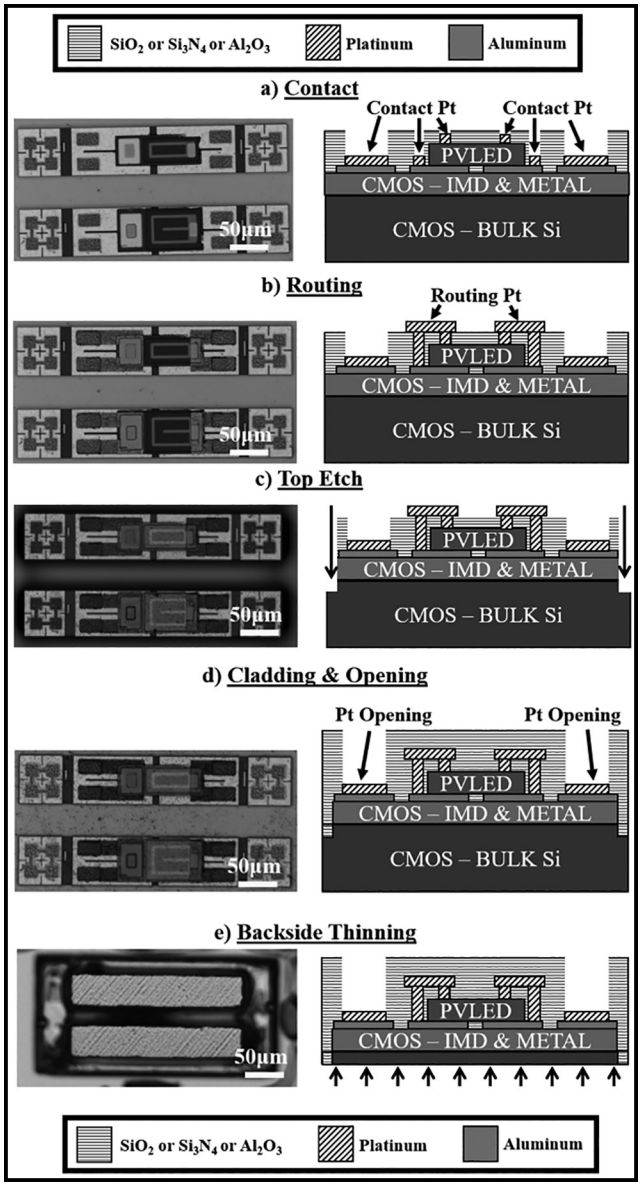

Figure 2: Fabrication flow of MOTE integration where AlGaAs PVLED is integrated on CMOS [6].

Wide-Bandgap p-Channel Transistors Based on GaN/AlN

CNF Project Number: 2800-19

Principal Investigator(s): Debdeep Jena, Huili Grace Xing

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Primary Source(s) of Research Funding: Intel Corporation

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Primary CNF Tools Used: SC4500 evaporator, PT 770 ICP/RIE etcher

Abstract:

Wide-bandgap (WBG) p-channel transistors, which can be monolithically integrated with WBG *n*-channel transistors, are the missing piece to the construction of WBG CMOS circuitry, which could provide tightly-integrated control over power and RF electronics. This report demonstrates high on-current *p*-channel devices based on one of the most promising platforms: the GaN/AlN heterojunction.

Summary of Research:

Though gallium nitride (GaN) electronics have advanced rapidly over the last decade to become a major player in the RF and power electronics spaces, *p*-channel devices in GaN have proven difficult to produce. The low hole mobility, poor acceptor efficiency, and hard-to-contact deep valence bands have limited device performance. This highlight celebrates advances on this front achieved in the Cornell NanoScale Science and Technology Facility and reported at the 2019 International Electron Devices Meeting [1].

An epitaxial stack consisting of a p^{++} InGaN cap on a GaN channel on an AlN buffer was grown by molecular beam epitaxy. Pd/Ni ohmic contacts were formed by e-beam evaporation in an SC4500 evaporator. After mesa isolation, the contacts were used as a mask to perform a global recess of the InGaN layer in the PT 770 ICP/RIE etcher. A SiO_2 hard mask was deposited using the Oxford 100 PECVD and patterned to reveal gate recess regions, which were then etched by the PT 770. After mask removal, the SC4500 evaporator was used to put down Mo/Au based gate contacts. All photolithography was performed in the GCA Autostep 200.

Finally, p-channel devices with 600 nm gate recess lengths were measured with up to 100 mA/mm on-current and 1-2 orders of on-off modulation, limited by the Schottky gate leakage. While this leaves significant room to improve upon the gating, the overall device performance compares well with the state-of-art in this field, as shown in Figure 1, demonstrating the promise of GaN/AlN based electronics for a wide-bandgap CMOS future.

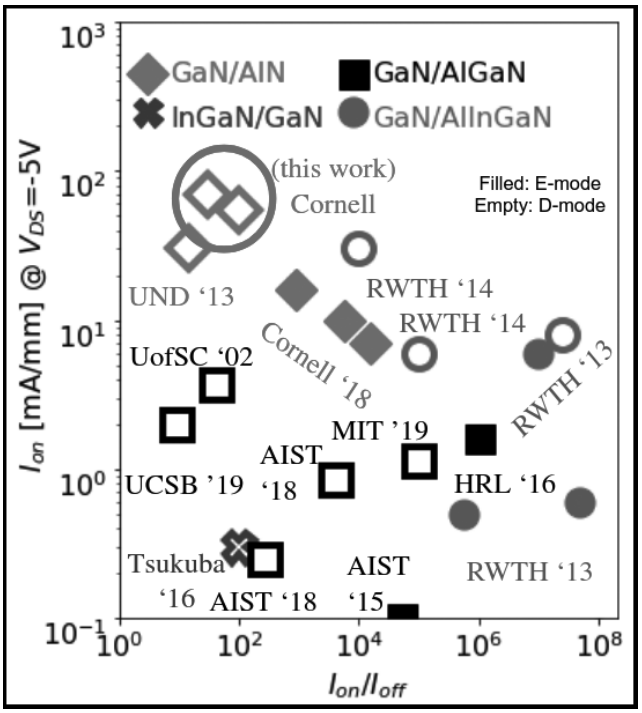

Figure 1: Current-levels and modulation ratios achieved for various p*-channel device demonstrations in the III-Nitrides. Noting that this is a rapidly advancing field, it is critical to timestamp this benchmark as drawn from only the publicly available literature as of July 2019. It is seen that GaN/AlN devices enable some of the highest on-currents possible. (See pages vi-vii for full color version.)*

References:

[1] S. J. Bader, et al., "GaN/AlN Schottky-gate p-channel HFETs with InGaN contacts and 100 mA/mm on-current," in International Electron Devices Meeting. DOI: 10.1109/IEDM19573.2019.8993532 (2019).

T-Gated AlN/GaN/AlN HEMTs with I_D > 3 A/mm, f_{max} = 230 GHz

CNF Project Number: 2800-19

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Primary Source(s) of Research Funding: Semiconductor Research Corporation

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Primary CNF Tools Used: AFM, i-line stepper, PT770 etcher, Oxford 81 etcher, odd hour e-beam evaporator, JEOL 6300 EBL, Oxford PECVD, AJA sputter deposition, Woolam ellipsometer, Zeizz Ultra SEM, Leica critical point dryer, Glen1000 resist stripper, P7 profilometer

Abstract:

In this work, we report record on-current and f_t/f_{max} product for the AlN/GaN/AlN HEMT. The devices demonstrated record on-currents over 3 A/mm with an on-resistance of 1 Ω·mm and excellent saturation. Transfer characteristics revealed I_{on}/I_{off} ratio of 10^3 and peak transconductance of 0.6 S/mm. Bias-dependent S-parameters were measured in the range of 0.05-40 GHz. The extracted f_t/f_{max} = 132/233 GHz (L_G = 45 nm) is the highest f_t/f_{max} product reported on the AlN platform.

Summary of Research:

Next-generation (6G) wireless communication and high-resolution radar systems target high-power operation in the terahertz regime. Gallium nitride high-electron-mobility transistors (GaN HEMTs) are well-suited for this high-power, high-frequency application. However, the conventional AlGaN/GaN heterostructure provides poor quantum confinement of the two-dimensional electron gas (2DEG), generating short channel effects at high frequencies. Additionally, its RF power performance is limited by the breakdown voltage. The AlN/GaN/AlN heterostructure offers material and device design advantages over the conventional AlGaN/GaN HEMT: the AlN buffer tightly confines the 2DEG and offers a higher thermal conductivity path than a thick GaN buffer, and the AlN barrier induces higher density 2DEGs at thinner distances (5 nm). AlN also maximizes the barrier bandgap, improving breakdown voltage.

Recently, fully realized T-gated AlN/GaN/AlN HEMTs were fabricated and characterized. The T-gates were defined via electron-beam lithography using a trilayer resist stack, and Ni/Au (50/200 nm) gate metal was deposited via e-beam evaporation. The resulting structure is shown in Figure 1.

The devices demonstrated record on-currents over 3 A/mm with an on-resistance of 1 Ω·mm and excellent saturation. Transfer characteristics revealed I_{on}/I_{off} ratio of 10^3 and peak transconductance of 0.7 S/mm. All DC characteristics are shown in Figure 2.

Bias-dependent S-parameters were then measured in the range of 0.05-40 GHz. The system was de-embedded via a short-open-load-through (SOLT) impedance standard substrate and on-wafer open/short structures. The device measured for dispersion also demonstrated f_t = 123 GHz, f_{max} = 233 GHz, as shown in Figure 3. This is the highest f_{max} reported for devices on the AlN/GaN/AlN heterostructure, and can be attributed to the incorporation of the T-gate geometry.

This excellent combination of on-current and f_{max} demonstrates the exciting potential for HEMTs on the AlN platform to enable the next generation of high-power, mm-wave communication.

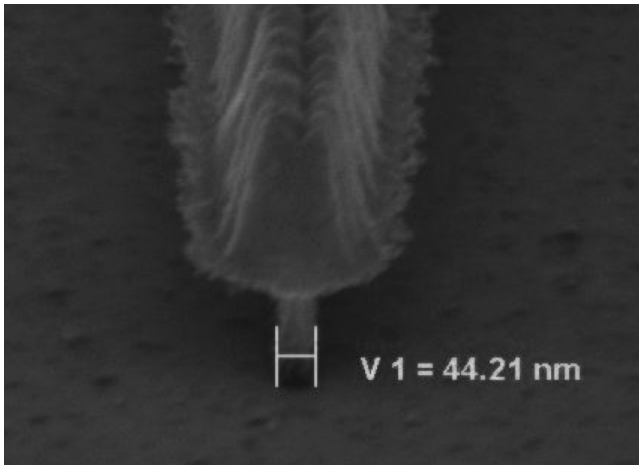

Figure 1: T-gate demonstrating a gate length of 44 nm.

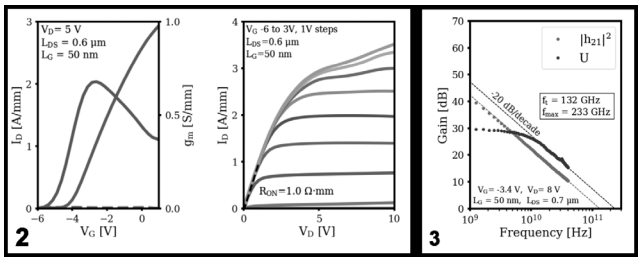

Figure 2, left: *DC characteristics for AlN/GaN/AlN HEMT.* ***Figure 3, right:*** *Small signal characteristics for the T-gated AlN/GaN/AlN HEMT.*

Ultra-Wide Bandgap Power Electronic Devices

CNF Project Number: 2800-19

Principal Investigator(s): Huili Grace Xing

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Primary Source(s) of Research Funding: NSF DMREF Program under Grant 1534303, AFOSR under Grants FA9550-17-1-0048, FA9550-18-1-0529 and FA9550-18-1-0479

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Primary CNF Tools Used: Oxford PECVD, Oxford ALD, odd-hour and even-hour evaporator, AJA sputtering tool, PT-770 etcher, Oxford 81 etcher, Gen-1000 etcher, UV-Ozone, Autostep i-line stepper, ABM contact aligner, Heidelberg mask writer-DWL2000, AFM-Veeco Icon, Oxford ALD FlexAL

Abstract:

Ultra-wide bandgap semiconductor materials, such as beta-phase gallium(III) trioxide (Ga_2O_3), have unprecedentedly high breakdown electric field, thus are considered very promising for use in power electronic devices. Through ingenuous design of the device structure and material interface, we successfully demonstrated high-voltage, low-loss vertical Ga_2O_3 Schottky barrier diodes and fin transistors with record-high performance. The device breakdown voltage shows a significant improvement with the employment of the field-plate technique as edge termination.

Summary of Research:

Beta-phase Ga_2O_3 has been under intensive research as a promising ultrawide-bandgap semiconductor material. It is expected to have a high breakdown electric field of up to 8 MV/cm due to the sizable bandgap of 4.5-4.7 eV, as well as a decent electron mobility of up to ~ 200 $cm^2/V{\cdot}s$. These properties yield a Baliga's power figure-of-merit higher than GaN and 4H-SiC, thus making Ga_2O_3 a strong material candidate for high power devices. In addition, melt-growth techniques for Ga_2O_3 substrates are available, which promises a cost-effective device platform.

Previously, we have successfully demonstrated Ga_2O_3 trench Schottky barrier diodes with a breakdown voltage (BV) of 2.44 kV [1]. In addition, we realized enhancement-mode vertical fin transistors with a breakdown voltage over 1 kV [2]. Despite the promising performance, the figure-of-merit of the previous devices are still far from the material limit of Ga_2O_3. One of the major reasons is the electric field crowding at the edge of the devices, which leads to premature breakdown. In this work, we improved upon the previous devices by adopting the field plate technique for more effective edge termination.

The fabrication process flow of the field-plated trench Schottky barrier diode prior to the addition of the field plate is largely the same as reported previously. The vertical fin channels were first formed by dry etching using PT-770 etcher. Then, Ti/Au (75/150 nm) cathode ohmic contact was deposited by e-beam evaporation, followed by the deposition of the first Al_2O_3 dielectric of 105 nm by atomic layer deposition using the Oxford ALD tool. After opening of the Al_2O_3 on top of the fin channel by dry etching, Ni (30 nm) Schottky contact and then Ti/Pt (40/40 nm) sidewall coverage were deposited by electron-beam evaporation and sputtering, respectively. To form the field plate, a second ALD Al_2O_3 dielectric layer of 125 nm was deposited. Then, contact holes were formed by dry etching to expose the anode metal. Lastly, the Ti/Al/Cu/Au (10/70/10/60 nm) field-plate metal stack was deposited.

The fabrication process for the field-plated Ga_2O_3 vertical fin transistors is as follows: An n^+ layer was formed on the top surface by Si-implantation and activated at 1000°C to facilitate the source ohmic contact. Submicron fin channels were defined by electron beam lithography and formed by dry etching using a BCl_3/Ar mixture. The resultant fin channels have a near vertical sidewall profile. After dry etching, the Cr/Pt etch mask was removed by Cr etchant and the wafer was treated with HF for 23 min to remove plasma damage. Next, the drain contact (Ti/Au) was deposited before the deposition of the gate stack, consisting of a 35 nm Al_2O_3 gate dielectric by atomic layer deposition (ALD) and a 50-nm Cr gate by sputtering. The gate stack and thick ALD Al_2O_3 spacer was patterned by photoresist planarization and

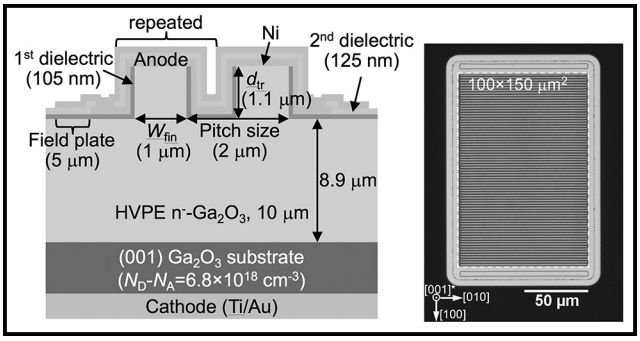

Figure 1: Schematic cross-section and optical top view of the field-plated Ga_2O_3 trench Schottky barrier diodes.

self-aligned etching processes detailed in our previous reports. The source electrode (Ti/Al/Pt) was deposited by sputtering after the spacer formation, simultaneously forming the source-connected field-plate.

The field-plated trench Schottky barrier diodes have a specific on-resistance of 10.5 mΩ·cm². In comparison with the regular SBDs, the field-plated trench SBDs have much lower leakage current as well as a much higher breakdown voltage of 2.89 kV. With addition of the field plate, the destructive breakdown voltage increases by ~ 500 V.

The field-plated trench SBD in this work achieves a power figure-of-merit (BV^2/R_{on}) of 0.80 GW/cm² from DC measurements, which is the highest among all Ga_2O_3 power devices to date [3].

The vertical Ga_2O_3 fin transistors exhibit normally-off operation and a threshold voltage of 1.8 V with a fin channel width of 0.15 μm. The device has an on-off ratio of > 10^8 and a V_{th} of ~ 1.8 V at 0.1 A/cm². The R_{on} is determined to be 25.2 mΩ·cm² from DC measurements. The field-plate helps boost the 3-terminal breakdown voltage from 1 kV to over 2.6 kV, a record high among all Ga_2O_3 transistors [4].

In summary, we have demonstrated improved performance in Ga_2O_3 power diodes and transistors, by using a field-plate technique, marking a significant step forward in the development of high performance Ga_2O_3 power transistors.

References:

[1] W. Li, Z. Hu, K. Nomoto, R. Jinno, Z. Zhang, T. Q. Tu, K. Sasaki, A. Kuramata, D. Jena, and H. G. Xing, 2018 IEEE International Electron Devices Meeting (IEDM), pp. 8.5.1, 2018.

[2] Z. Hu, K. Nomoto, W. Li, N. Tanen, K. Sasaki, A. Kuramata, T. Nakamura, D. Jena, and H. G. Xing, IEEE Electron Device Lett. 39, 869 (2018).

[3] W. Li, K. Nomoto, Z. Hu, D. Jena, and H. G. Xing, IEEE Electron Device Lett. 41, 107 (2020).

[4] W. Li, K. Nomoto, Z. Hu, T. Nakamura, D. Jena, and H. G. Xing, 2019 IEEE International Electron Devices Meeting (IEDM), pp. 12.4.1, 2019.

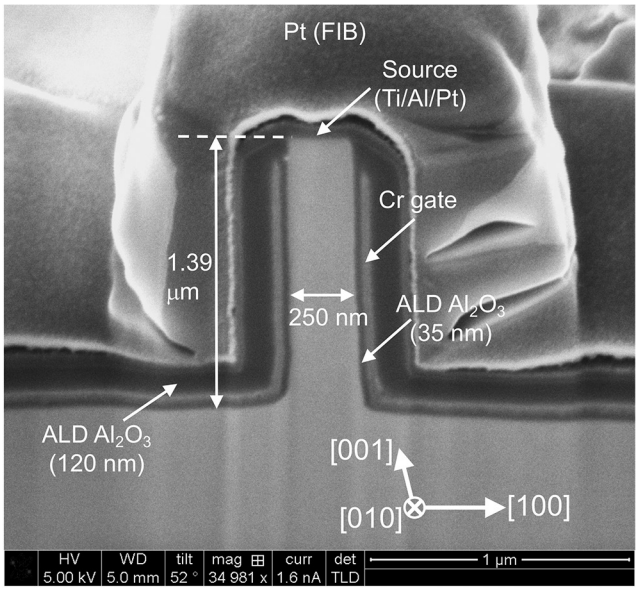

Figure 2: SEM cross-section of the field-plated Ga_2O_3 vertical fin transistors.

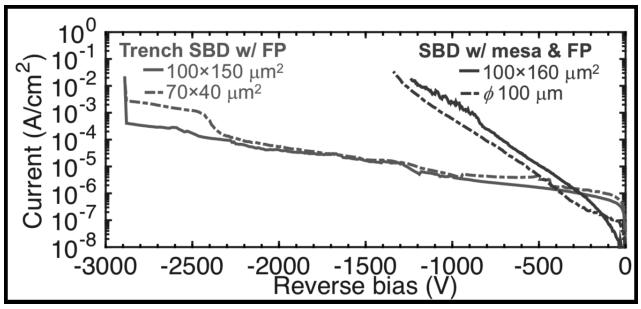

Figure 3: Reverse I-V characteristics of the field-plated Ga_2O_3 trench Schottky barrier diodes.

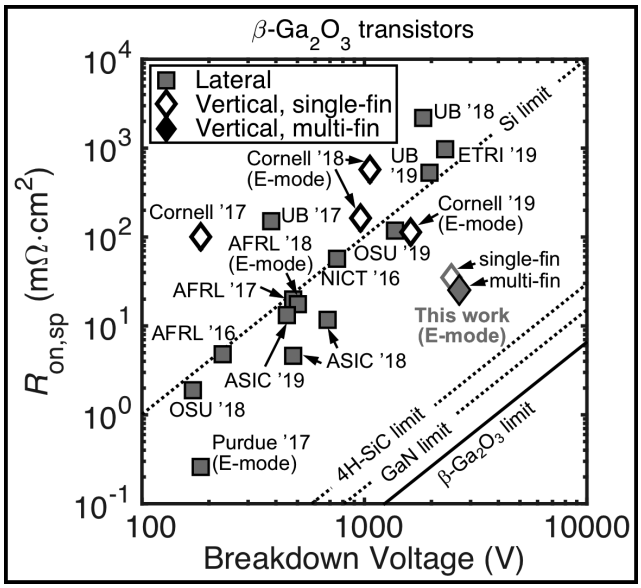

Figure 4: Performance of the field-plated vertical fin transistors in comparison with literature reports.

InAlN/GaN HEMTs on Si with Regrown Contacts and f_T/f_{MAX} of 250/204 GHz

CNF Project Number: 2800-19

Principal Investigator(s): Huili Grace Xing, Debdeep Jena

User(s): Kazuki Nomoto, Lei Li, Austin Hickman

Affiliation(s): School of Electrical and Computer Engineering, Cornell University

Primary Source(s) of Research Funding: ComSenTer

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Primary CNF Tools Used: Autostep i-line stepper, Heidelberg mask writer DWL2000, P7 profilometer, FilMetrics, AFM Veeco Icon, Zeiss SEM, PT770, Oxford 81, Oxford PECVD, Oxford ALD, SC4500 evaporators, AJA sputter deposition tools, RTA AG610, JEOL 9500

Abstract:

Depletion-mode high-electron mobility transistors (HEMTs) based on a quaternary barrier $In_{0.17}Al_{0.83}N$/AlN/GaN heterostructure on Si substrate were fabricated. The 55 nm long gate device shows a DC drain current density of 2.8 A/mm, a peak extrinsic transconductance of 660 mS/mm, and balanced current gain cutoff frequency f_T and maximum oscillation frequency f_{MAX} are 250 and 205 GHz, respectively.

Summary of Research:

Gallium nitride high electron mobility transistors (GaN HEMTs) have high breakdown voltages, high two-dimensional electron gas (2DEG) densities, and a high electron saturation velocity. These properties make them ideal for high-power and high-frequency applications, such as switches in power systems and amplifiers in wireless communication systems.

To date, the highest speed GaN HEMTs are demonstrated on SiC substrates, all of which employ regrown ohmic contacts to minimize source/drain resistances. In this report, we have demonstrated the high-frequency and high-power performance capacity of GaN HEMTs on Si substrates. The $I_{D,MAX}$, peak g_m and f_T-f_{MAX} product are among the best reported for GaN HEMTs on Si, which are very close to the state-of-the-art depletion-mode GaN HEMTs on SiC without a back barrier. This highlight celebrates advances on this front achieved in the CNF and published at IEEE Electron Devices Letters [1].

The InAlN/AlN/GaN HEMT structure consists of a 10 nm $In_{0.17}Al_{0.83}N$ barrier, a 1 nm AlN spacer (total barrier thickness: 11 nm), an 800 nm unintentionally doped GaN channel, and AlGaN/AlN buffer and nucleation layers on 200-mm-diameter Si substrate, grown by a Propel® HVM MOCVD system at Veeco Instruments. Room temperature Hall-effect measurements prior to device fabrication showed a 2DEG sheet concentration of 2.27×10^{13}/cm^2 and electron mobility of 1430 cm^2/V·s, corresponding to a sheet resistance of 206 Ω/sq.

A schematic cross-section of the InAlN/AlN/GaN HEMT device with regrown n$^+$ GaN contacts is shown in Figure 1(a). The device fabrication process started with patterning of a SiO_2 mask for n$^+$GaN ohmic regrowth by PA-MBE. The preregrowth etch depth into the HEMT structure was 40 nm, and regrown n$^+$GaN was 100 nm with a Si doping level of 7×10^{19} /cm^3. Non-alloyed ohmic contact of Ti/Au/Ni was deposited by e-beam evaporation. T-shaped Ni/Au (40/200 nm) gates were formed by electron-beam lithography by JEOL 9500, followed by liftoff. TLM measurements yielded a contact resistance of 0.07 Ω·mm. The device presented here has a regrown n$^+$GaN source-drain distance L_{sd} of 175 nm, a gate width of 2 × 25 μm, and a gate length L_g of 55 nm. Figure 1(b) shows an angled-SEM image of the fabricated InAlN/AlN/GaN HEMT.

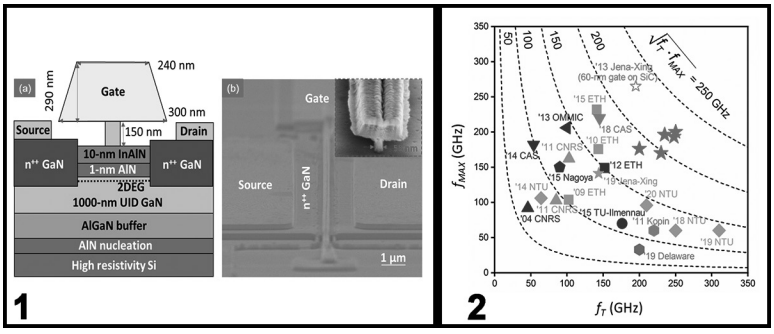

Figure 1, left; *(a) Schematic cross-section of InAlN/AlN/GaN HEMTs on Si with regrown n$^+$GaN contacts. (b) An angled SEM image of a fabricated InAlN/AlN/GaN HEMT with an EBL T-gate.* ***Figure 2, right:*** *Comparison of the measured f_T and f_{MAX} of GaN HEMTs on Si substrates. (See pages vi-vii for full color versions.)*

The observed maximum drain current $I_{D,MAX}$ of 2.8 A/mm and the on resistance R_{ON} of 0.6 Ω·mm, along with the peak transconductance g_m of 0.66 S/mm, are among the best in GaN HEMTs on Si, comparable to GaN HEMTs on SiC without a back barrier. At low V_{DS}, these HEMTs typically exhibit a decent I_{ON}/I_{OFF} ratio ~ 10^5; HEMT A has the highest gate leakage among all the tested devices, most likely due to processing non-uniformity. The f_T/f_{MAX} of 250/204 GHz are obtained after de-embedding in HEMT A; in comparison, neglecting the short de-embedding test structure renders similar f_T/f_{MAX} values of 245/187 GHz. In Figure 2, the f_T and f_{MAX} values achieved in this work are compared to other reported GaN HEMTs on Si, as well as the state-of-the-art GaN HEMTs on SiC with similar epi-structures and device dimensions (gate length, barrier materials, and its thickness, no back barrier). It can be seen the present HEMTs are clustered near the upper right corner as desired, with $(f_T \cdot f_{MAX})^{1/2}$ very close to that of the GaN HEMTs on SiC with a comparable gate length.

GaN HEMTs on Si with different geometries were fabricated, measured, and analyzed. The analysis confirms the benefits of n^{++}-GaN source/drain contacts and T-shaped gates, especially in achieving both high f_{MAX} and f_T. With the state-of-the-art regrown ohmics, scaled source-drain separation and T-gates, GaN HEMTs on Si achieve comparable metrics with that on SiC in terms of DC and small-signal performance.

References:

[1] L. Li, K. Nomoto, D. Jena, H. G. Xing, et al., "GaN HEMTs on Si with Regrown Contacts and Cutoff/Maximum Oscillation Frequencies of 250/204 GHz"; IEEE Electron Device Lett., 10.1109/LED.2020.2984727, March. 2020.

Quantum Materials and Technologies

CNF Project Number: 2803-19

Principal Investigator(s): Huili Grace Xing, Debdeep Jena

User(s): John Wright, Zexuan Zhang, Jashan Singhal, Hyunjea Lee, Joseph Casamento

Affiliation(s): Materials Science and Engineering, Electrical and Computer Engineering; Cornell University

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Primary CNF Tools Used: Autostep 2000 i-line stepper, JEOL 6300, AJA sputter, Veeco AFM, PT-770 etcher, Oxford 81 etcher

Abstract:

The integration of new material properties into electronics devices creates new possibilities for device performance, architecture, and function. We therefore investigate the fabrication and applications of materials with exceptional properties, including superconductivity, ferromagnetism, ferroelectricity, and topologically non-trivial electronic states.

Summary of Research:

With a sizable bandgap higher than that of silicon, two-dimensional (2D) layered materials can be potential candidates for high voltage applications. One of 2D materials, WSe_2 is used for enhancement mode p-channel field effect transistors (FETs) for high voltage devices, being patterned by JEOL 6300 in CNF. Ambipolar transport in back-gate WSe_2 FETs is often reported in literature, which is a feature of junction-less transistors. However, the breakdown voltage of back-gate WSe_2 FETs with overlapping source and drain is found to be limited by the ambipolar transport. In the off-state of WSe_2 p-FETs, the voltage across the overlapping drain and gate creates an electron channel near the drain; electrons are then injected from the drain contact into the electron channel by tunneling and swept to the source by a lateral electric field across the channel, generating high off-state leakage currents. This ambipolar-limited breakdown is confirmed by depositing Al_2O_3, which introduces interface states near the conduction band edge of WSe_2, and the electron current is suppressed since the drain-gate voltage is not able to raise the Fermi-level into the conduction band. With the suppression of the ambipolar transport, WSe_2 p-FETs show improved breakdown voltages up to -100 V (Figure 1), corresponding to a critical electric field in WSe_2 higher than 200 kV/cm.

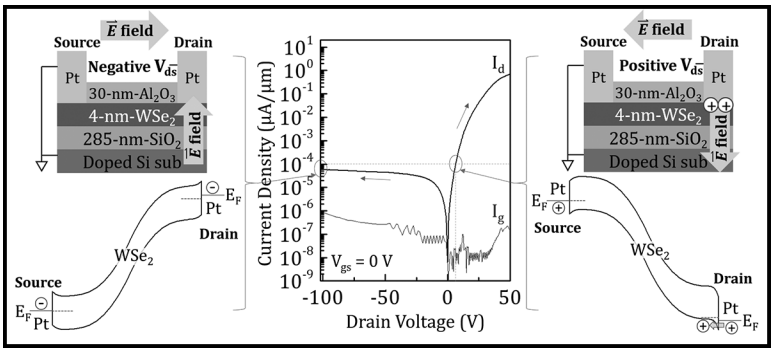

Figure 1: Off-state leakage currents and corresponding energy band diagram cartoons of the WSe_2 p-FET.

Epitaxial ferroelectric semiconductor devices have promise in applications of low power transistors and nonvolatile memories. Their realization has been largely hindered due to material development issues. Our goal was to utilize a novel epitaxial ferroelectric material system, $LuFeO_3$, integrated on GaN to achieve an epitaxial ferroelectric semiconductor field-effect transistor (FE-FET). With the utilization of CNF equipment such as the SC4500 odd hour electron beam evaporator, AG 610 rapid thermal annealer, AJA ion mill, Veeco Dimension Icon atomic force microscope, and GCA Autostep 200 DSW i-line wafer stepper, we have taken the steps toward achieving that goal.

$LuFeO_3$ is intended to act as a ferroelectric gate dielectric and a two-dimensional electron gas (2DEG) formed from a conduction band offset at the $Al_{0.25}Ga_{0.75}N$-GaN interface serves as the semiconductor electron channel.

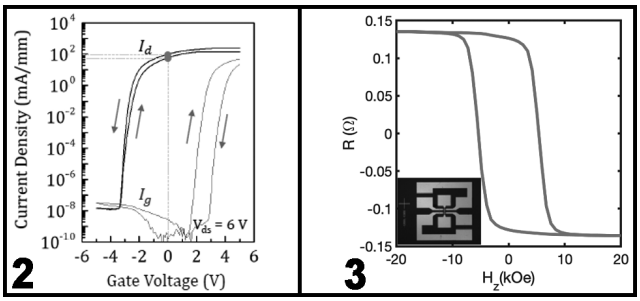

Figure 2, left: I_d-V_{gs} and I_d-V_d characteristics of the $LuFeO_3$-GaN Fe-FET device, showing 2DEG depletion and hysteretic behavior, as well as saturation. Figure 3, right: Hall resistance of Pt/Mn_4N Hall bar (Inset: photo of the measured device).

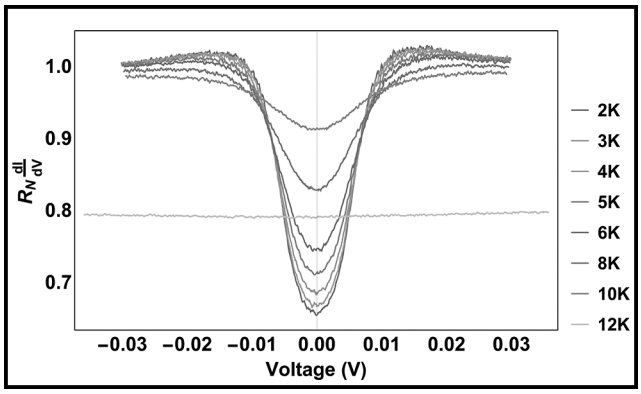

Figure 4: Differential conductance of a NbN/2DEG/NbN device fabricated using a nitrogen polar GaN/AlN quantum well. (See pages vi-vii for full color version.)

Drain current, gate voltage (I_d-V_{gs}) electrical data show a high on-off ratio (10^6) and depletion of the 2DEG in the negative bias regime with counterclockwise hysteretic behavior (Figure 2). These results show effective device patterning, etching, and electrical contact to the electron channel. This is a significant step toward a Fe-FET involving $LuFeO_3$-GaN based heterostructures.

Seamless integration of ferromagnet on semiconductor such as GaN is a promising route towards future energy efficient applications because it provides the unique opportunity to merge memory and logic components. To this end, we have focused on the epitaxial integration of various magnetic phases of MnxNy with wide bandgap semiconductors (GaN and SiC) [1]. Ferrimagnetic Mn_4N layers were grown using molecular beam epitaxy technique on different substrates including cubic MgO, $SrTiO_3$ and hexagonal GaN, SiC. Structural and magnetic characterization was done with the help of various CNF tools and they were found to differ significantly on different substrates [2]. Particularly, Mn_4N layers grown on MgO exhibits strong perpendicular magnetic anisotropy (PMA) and smooth surface.

For spintronic applications based on spin orbit torque (SOT), heavy metal Pt was sputtered on MBE grown Mn_4N and further patterned into test structures such as Hall bars through photolithography, ion mill and lift off process. An image of the patterned structure could be seen in inset of Figure 3.

Transport properties were measured on patterned devices where a square hysteresis loop in field dependent Hall resistances was observed (Figure 3). Such hysteresis loop is typical of a PMA magnetic thin film with high structural quality. At this stage, however, SOT switching of Pt/Mn_4N hasn't been demonstrated, possibly due to (1) poor interface quality between Pt and Mn_4N caused by air exposure or (2) insufficient spin injection considering the large strength of PMA in Mn_4N. Future steps would include optimizing Pt/Mn_4N structure along these directions.

Topological superconductivity can be engineered by utilizing topologically trivial S-wave superconductors to induce correlated electronic states in non-superconducting topological electronic systems, such as the quantum Hall state in high mobility two-dimensional electron gases (2DEG). To explore these phenomena we have grown epitaxial nitride superconductor/semiconductor heterostructures utilizing nitrogen polar GaN/AlN quantum wells with superconducting NbN contacts. The structure places the 2DEG in closer proximity to the surface then would be the case with the more conventional metal-polar nitride AlN/GaN quantum well, while also reducing the tunneling barrier between the superconducting top contact and the 2DEG. Once the structure is grown by MBE the NbN is selectively etched to create devices wherein the 2DEG in the GaN quantum well forms a conducting channel with NbN contacts.

Figure 4 shows the differential conductance of a NbN/2DEG/NbN device at temperatures around the superconducting transition temperature of the NbN film, which is approximately 12K. We see evidence that below 12K the 0V differential conductance is reduced, which is due to the opening of an energy gap at the fermi level in the NbN.

Further work will focus on placing the 2DEG in even closer proximity to the superconductor to increase the proximity induced correlated states, which will be evidenced by an increase in the 0V differential conductance.

References:

[1] S. Dhar, et al. Appl. Phys. Lett. 86, 112504 (2005).

[2] Z. Zhang, et al. AIP Advances 10, 015238 (2020).

Neural Probe Utilizing Micro-Coil Magnetic Stimulation with CMOS Technology Integration for Spatially Programmable Neurostimulation

CNF Project Number: 2847-19

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User(s): Edward Szoka

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Primary CNF Tools Used: Oxford ALD FlexAL, AJA sputter deposition, ABM contact aligner, Unaxis 770, PT770 etcher, Oxford 100

Abstract:

Neural prostheses have been effective in treating neurological disorders using electrical stimulation through micro-electrodes [1]. However, micro-electrode neurostimulation suffers from the inability to selectively activate neurons based on orientation [2] as well as maintaining long-term functionality [3]. Magnetic stimulation produced by micro-coil devices avoid these issues as the induced electric fields are asymmetric and magnetic fields can pass through biological materials allowing for complete encapsulation [4,5]. Mixed-signal circuitry is integrated into the proposed micro-coils by fabricating the design in a 180 nm CMOS technology process. Further nanofabrication techniques are applied to release the proposed micro-coils from the original chip packaging to produce a neural probe with spatially programmable micro-coil magnetic stimulation sites. Preliminary *in vitro* patch-clamp recordings of retinal tissue with programmed micro-coil magnetic stimulation sites has shown controlled neural behavior. Further research exploring the programmable stimulation site regions are ongoing.

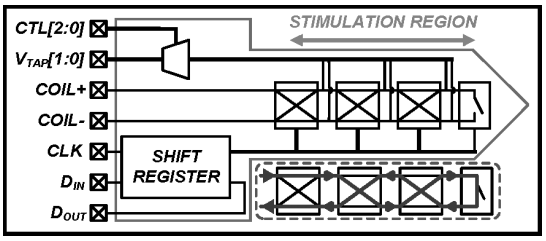

Figure 1: High-level diagram of the proposed programmable micro-coil neural probe with an example of programmed current direction.

Summary of Research:

The proposed micro-coil system is shown in Figure 1. The programmable stimulation sites are implemented by using a programmable switching network to direct the micro-coil current flow. The switching network can be programmed into four states: pass straight through, cross over, short-circuit, or open-circuit. The switches are implemented as pass gates with the NFETs sized at W/L of 1.5 mm/180 nm and PFETs sized at W/L of 2 mm/180 nm. The switches are sized to have a maximum resistance of 2W. With the trace resistance approximately 4W, the maximum coil resistance is 18W, allowing safe operation of the FETs while driving the micro-coil with 100 mA of current. The micro-coil is programmed using a shift register where the programming bits are buffered and routed down the probe to the switching networks. For electrical verification the coil segments are broken out to a multiplexer and brought off-chip to validate the current direction based off the voltage drop throughout the micro-coil.

The micro-coils are released and thinned down from the original chip packaging through a series of nanofabrication steps. Aluminum oxide and chrome are deposited (to serve as silicon etching and oxide etching masks respectively) and patterned using conventional photolithography and a combination of wet-etch and plasma etching. The oxide is etched in a CHF_3/O_2 oxide plasma etch using the Oxford 100 to expose the silicon surface. The exposed topside silicon is etched in the Unaxis 770 using a deep reactive-ion etching (DRIE) process down to the desired thickness of the neural probe (75 μm). The chips are flipped upside-down and the bulk silicon is etched in the same DRIE process until the micro-coils are released from the rest of the chip. The nanofabrication process to release the micro-coils is shown in Figure 3. The released micro-coils are then wire bonded to a carrier PCB, the wire bonds are protected with epoxy, and the entire assembly is coated with around 2 μm of Parylene-C to further encapsulate the micro-coil.

The micro-coils were fabricated in a 180 nm 1P6M CMOS process with a probe length and width of 1.9 mm and 0.1 mm respectively. A micrograph and scanning electron microscope (SEM) image of the micro-coil is shown in Figure 3.

Preliminary biological testing has been done using a patch clamp recording electrode in conjunction with the micro-coil in mouse retinal tissue. The recorded neuron was located at the tip of the micro-coil probe. Stimulation trials were done by driving the micro-coil with twenty ramp current waveforms spaced 200 ms apart. Figure 4 shows the neural response of the clamped neuron at the first and fourth stimulation sites (next to the neuron and 750 µm away). The data shows that stimulation near the neuron elicited indirect stimulation as there was immediate suppression of neural activity for 100 ms followed by a spike train for all twenty stimulation pulses. Stimulation further away from the neuron showed neural behavior that was more akin to natural behavior than evoked responses.

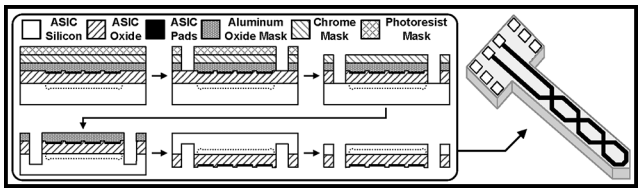

Figure 2: Nanofabrication process to release the micro-coils from the rest of the chip. Mask layers that are no longer being used are etched away between the shown process steps.

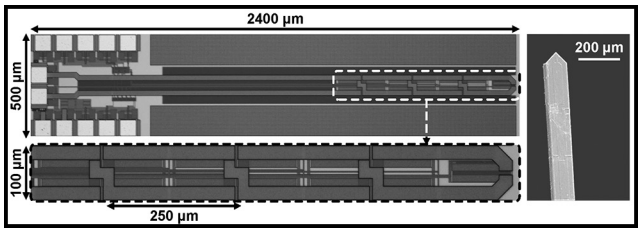

Figure 3: Unreleased micro-coil die photo with enhanced view of the stimulation region as well as an SEM image of a released micro-coil.

Conclusions and Future Steps:

Through the use of CMOS technology and nanofabrication techniques an insertable neural probe utilizing micro-coil magnetic stimulation with spatially programmable stimulation sites has been created. Preliminary biological testing with patch clamp measurements has shown repeatable evoked neural responses, however further testing utilizing a multi electrode array needs to be done to characterize the stimulation site regions. Future designs are also being created to utilize micro-coils with more turns to decrease the necessary stimulation current as well as incorporating current driving circuitry to independently drive each micro-coil.

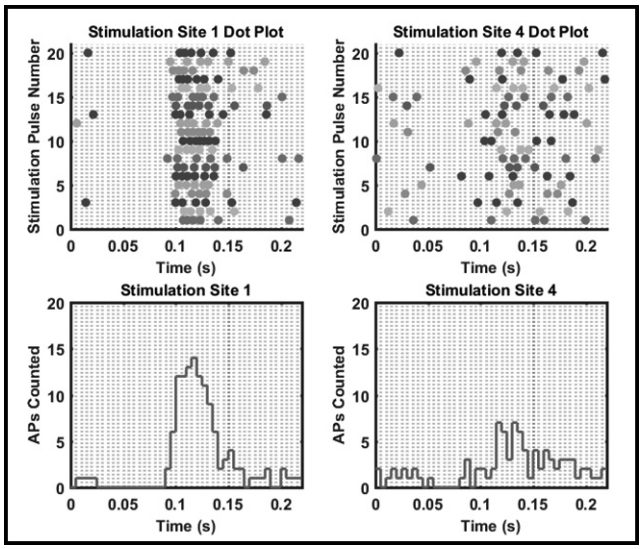

Figure 4: Dot plot and action potential count of patch clamp measurements from one neuron during stimulation at two different programmed sites. (See pages vi-vii for full color version.)

References:

[1] S. J. Bensmaia and L. E. Miller, "Restoring sensorimotor function through intracortical interfaces: progress and looming challenges," Nature Reviews Neuroscience, vol. 15, no. 5, pp. 313-325, 2014.

[2] M. H. Histed, V. Bonin, and R. C. Reid, "Direct activation of sparse, distributed populations of cortical neurons by electrical microstimulation," Neuron, vol. 63, no. 4, pp. 508-522, 2009.

[3] V. S. Polikov, P. A. Tresco, and W. M. Reichert, "Response of brain tissue to chronically implanted neural electrodes," Journal of Neuroscience Methods, vol. 148, no. 1, pp. 1-18, 2005.

[4] S. W. Lee, F. Fallegger, B. D. F. Casse, and S. I. Fried, "Implantable microcoils for intracortical magnetic stimulation," Science Advances, vol. 2, no. 12, 2016.

[5] S. W. Lee, K. Thyagarajan, and S. I. Fried, "Micro-coil design influences the spatial extent of responses to intracortical magnetic stimulation," IEEE Transactions on Biomedical Engineering, vol. 66, no. 6, pp. 1680-1694, June 2019.