

A 3D Circuit QED Architecture with Separate Readout and Coupling Cavities

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Abstract:

This work presents the development of a three dimensional circuit quantum electrodynamics (3D cQED) architecture with separate cavities for inter-quantum bit (qubit) coupling and for qubit readout. Such a separation allowed for optimization of the cavities for their separate tasks, as opposed to the compromise necessary in single-cavity architectures. The device designed was a 3D analogue of a working multi-resonator, multi-transmon qubit device in standard, planar circuit QED. By switching from coplanar waveguide (CPW) resonators to 3D cavity resonators, we expected to attain significantly higher qubit and resonator coherence times (tens of microseconds), allowing realization of complex quantum computing algorithms, while retaining the virtue of physical scalability. The architecture pursued also included local flux tuning of qubit transition frequencies, necessary for control

of qubit-qubit interactions on nanosecond timescales. We present here the design, simulation and initial characterization of the first prototype.

Introduction:

The emergence of cQED as a leading paradigm for the solid-state realization of quantum information processing has inspired a slew of refinements on the basic topology, which uses CPW resonator(s) to couple to one or more qubits. One such refinement replaces the CPW resonator(s) with 3D superconducting cavity resonator(s), a change that improves coherence times. Another refinement introduces separate cavities for readout and for memory/coupling. A multi-cavity scheme allows for specialized tuning of qubit-cavity coupling strength, g . A high g is desired between the qubit and the dispersively coupled readout cavity in order to increase the distinction between the measurements corresponding to the two qubit states, translating to an increase in readout fidelity. However, such strong coupling between the qubit and the inter-qubit coupling cavity creates residual cross-coupling between qubits. If resonant gates are used, then this coupling can be decreased to mitigate these negative inter-qubit effects while still matching the gate times achieved with dispersive gates.

It was thus straightforward to combine the above two ideas and to conceive of a multi-resonator, multi-qubit 3D cQED architecture. It should be noted that any such architecture should ideally also include the flux bias lines needed to tune the qubit transition frequencies on nanosecond timescales, needed to realize multi-qubit gates. In this work, we made use of a transmon qubit consisting of two superconducting aluminium islands connected by two Josephson junctions, all on a sapphire substrate.

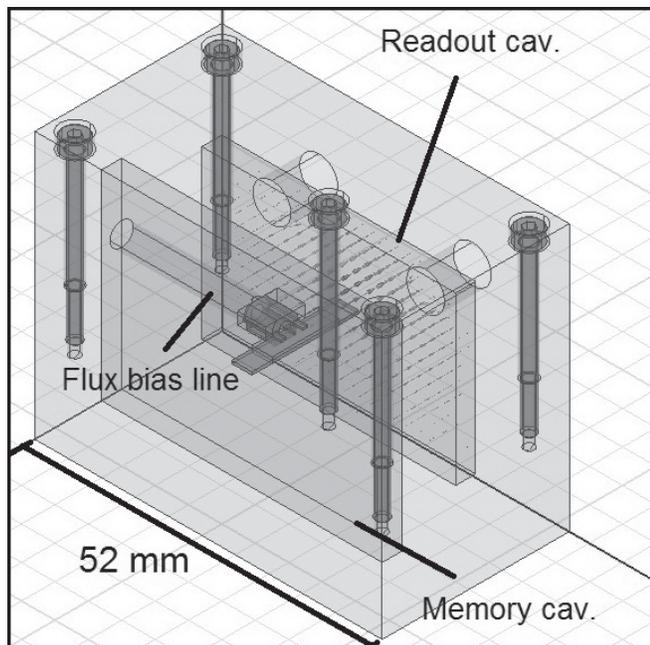


Figure 1: HFSS model of device geometry. The qubit substrate straddles the two cavities. The fundamental mode of the readout cavity is displayed as a vector plot.

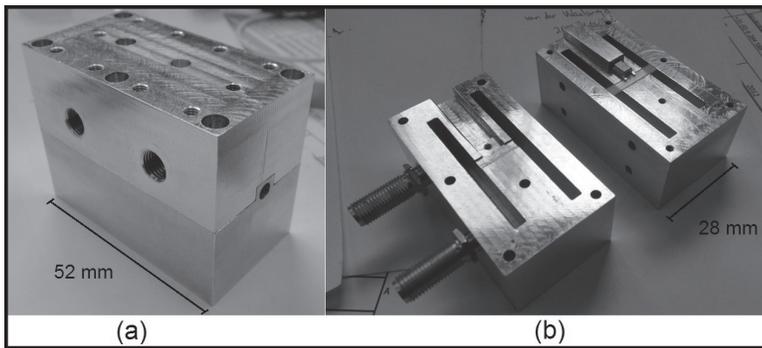


Figure 2: (a) Fabricated device, fully assembled.
(b) Fabricated device in two halves with connector/substrate visible.

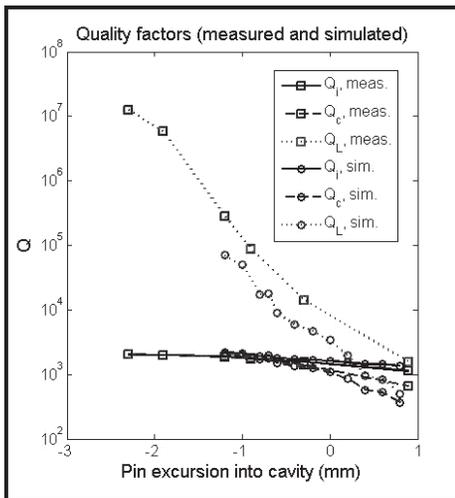


Figure 3: Loaded, intrinsic, and external quality factors as simulated and as measured. In simulation, zero dielectric loss is assumed, and the cavity is defined with bulk conductivity 3.8×10^7 S/m.

Design:

The cavity design was carried out primarily using ANSYS high frequency structure simulator (HFSS), a full wave simulator that allowed modeling of high-frequency electromagnetic behavior in arbitrary geometries. With HFSS, we could determine the geometries that provided the desired resonant frequencies and make predictions concerning the coupling and intrinsic quality factors of the individual cavities. Figure 1 displays the HFSS model for reference.

The qubit design was carried out using ANSYS Maxwell, a simulator geared towards electro- and magneto-static simulations. We employed it to calculate the inter-island capacitance of the qubit structure, a parameter that determines the charging energy of the qubit. Due to the device geometry, however, the physical size of the qubit was nearly a fifth of a wavelength at the highest operating frequency of interest. This implied that the super-conducting islands acted as distributed elements, rather than as lumped elements, casting some uncertainty on the simulation results.

Flux bias was controlled by applying a voltage between a shorted trace and ground, generating a current through the

trace that in turn gave rise to a magnetic flux normal to the plane of the trace. The use of very small profile connectors was necessary due to the relatively high (7 GHz) frequencies of operation of the device. We employed a standard miniature subminiature push-on (SMPM) edge launch connector to realize the connection of a coaxial cable to the trace on the substrate.

Fabricated Device:

The finalized design was sent to a professional rapid CNC prototyping company for manufacture in aluminium 6082-T651. Figure 2 depicts the fabricated device. In actual operation, the qubit and flux bias geometry will be fabricated on the displayed substrate, and the connector will be wirebonded to the flux bias geometry.

Experimental Results:

At this time, only room temperature measurements of transmission through the readout cavity have been made, varying coupling strength by using coupling pins of different lengths. Good qualitative agreement is seen between HFSS and measured results. Ten resonant modes of the readout cavity were observed and differed from those predicted by simulation by, at most, 150 MHz. The average deviation was 45 MHz, and the median deviation was 20 MHz. The desired resonant frequency for the fundamental mode of the readout cavity was 7 GHz; the observed value was 7.03 GHz. Figure 3 depicts measured and simulated quality factors for the readout cavity.

Conclusions:

A preliminary two-cavity one-qubit device has been fabricated, and initial characterization does not deviate significantly from predicted behavior. The next step is to characterize the device under superconducting conditions (i.e., low temperatures) and finalize/fabricate a qubit for this device. At this time, a scaled-up three-cavity two-qubit device has been fabricated, and future work will include realization of quantum algorithms with the benefits of this architecture.

Acknowledgements:

We would like to thank Dr. Leo DiCarlo for his role as principal investigator, Diego Ristè and Vishal Ranjan for helpful discussion, and Remco Roeleveld for final machining. We thank the entire QT team for their overall support, especially Hans Mooij for his role as our formal contact here. Finally, we thank the NNIN iREU Program and the NSF for their financial support.