Electrical Characterization of GaAs/InAs Core/Shell Nanowires and InAs Nanotubes

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Introduction:

Semiconductor nanowires (NWs) show promise for a variety of nanoelectronic applications due to their high surface area to volume ratio and two-dimensional confinement of charge carriers. The properties of these NWs can be further manipulated through the formation of radial heterostructures. In particular, the use of a gallium arsenide (GaAs) NW core to support an indium arsenide (InAs) shell can potentially result in a tubular conductor suitable for high performance field effect transistors (FETs). The GaAs core can later be removed by selective etching, resulting in an InAs nanotube. Due to its additional surface area and the relaxation of dislocations associated with the GaAs/InAs interface, it is expected that the mobility (μ_{FE}) of this InAs nanotube would exceed that of the core/shell NW. Here, we investigate and compare the resistivity (ρ), electron concentration (n_e), and μ_{FE} of GaAs/InAs core/shell NWs and InAs nanotubes.

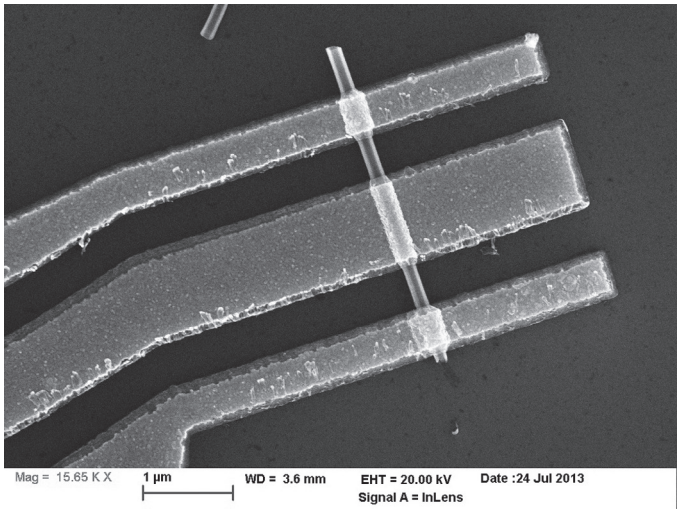

Figure 1: Top-view SEM image of an InAs nanotube FET.

Experimental Procedure:

The core/shell NWs studied were grown by molecular beam epitaxy as described by Rieger, et al. [1]. NWs were grown with three different core diameters/shell thicknesses: 110 nm/15 nm, 110 nm/22 nm, 150 nm/18 nm.

In order to extract ρ, n_e, and μ_{FE}, top-gate NW FETs were fabricated with hafnium oxide (HfO_2) as the gate dielectric and GaAs/InAs core/shell NWs as the channel. Core/shell NWs were first coated with 10 nm of HfO_2 by atomic layer deposition. The NWs were then mechanically transferred to a substrate consisting of 200 nm of silicon oxide on degenerately doped silicon.

Optical microscope images of the distribution of the transferred NWs were used to design source, drain, and top-gate contacts for selected NWs. Electron-beam lithography was used to define 1 μm long Ti/Au top-gates, which were deposited by electron beam evaporation. After gate deposition, the HfO_2 dielectric was removed from the source and drain regions of the NW using a three minute wet etch in 0.05% hydrofluoric acid. Source and drain contacts were then patterned and deposited in the same way as the top-gate contacts. The spacing between adjacent contacts was 500 nm. The electrical properties of the NWs were characterized by two-, three-, and four-probe current-voltage (I-V) measurements on the NW FETs.

After characterization of the core/shell NWs was complete, the GaAs core was selectively etched with a 1:1:40 mixture of NH_4OH:H_2O_2:H_2O for five minutes to obtain InAs nanotubes, while leaving the FETs intact. Electrical measurements were then repeated for the nanotube FETs. Scanning electron microscope (SEM) images of the nanotube FETs were taken after electrical characterization (Figure 1).

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Equation 1: $\rho = \frac{RA}{L}$

Equation 2: $C = \frac{2\pi\epsilon_0\epsilon_r L}{ln\left[\frac{t_{ox}}{r}+1+\sqrt{\left(\frac{t_{ox}}{r}\right)^2+2\frac{t_{ox}}{r}}\right]}$

Equation 3: $n_{el} = -\frac{CV_{th}}{eLA}$

Equation 4: $\mu_{FE} = \frac{g_m L^2}{V_{SD}C}$

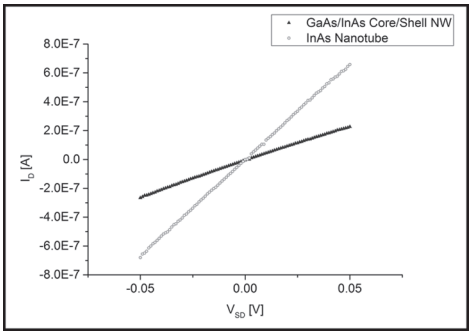

Figure 2: Exemplary two-probe I-V characteristics of a core/shell NW vs. nanotube.

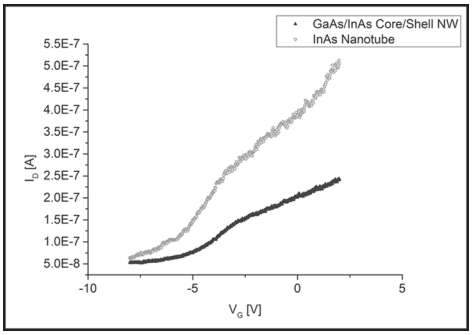

Figure 3: Exemplary three-probe ID-VG characteristics of a core/shell NW vs. nanotube.

The resistivity of each NW and nanotube was determined by two-probe measurements using Equation 1, where L is the length of the NW between source and drain, R is the resistance of the NW taken from the I-V curve, and A is the portion of the cross-sectional area of the NW that conducts, which is limited to the InAs shell in core/shell NWs due to the band alignment of GaAs and InAs [2]. A small number of four-terminal devices were fabricated to measure the contact resistance, which was found to be negligible in comparison to the resistance of the NWs and was not included in calculations of ρ.

Values for n_e and μ_{FE} were extracted from three-probe measurements according to Equations 3 and 4, where C is the gate capacitance, V_{th} is the threshold voltage from the I_D-V_G curve, e is the electron charge, g_m is the transconductance from the I_D-V_G curve, and V_{SD} is the voltage between the source and drain, which was held constant at 0.02 V for all three-probe measurements. The gate capacitance, C, was approximated using Equation 2, which is the general form of the gate capacitance for a back-gate NW FET, where ε_0 is the vacuum permittivity, ε_r is the relative permittivity of the gate oxide, t_{ox} is the gate oxide thickness, and r is the NW radius. To account for the use of a top-gate instead of a back-gate, the capacitance values calculated by Equation 2 were increased by 14%, as suggested in Dayeh et al. [3].

Results and Discussion:

For forty-one GaAs/InAs core/shell NWs tested, an average ρ of 0.14 Ω•cm was found. After etching of the NW cores to obtain InAs nanotubes, the average ρ decreased to 0.05 Ω•cm. An example of two-probe I-V curves for one device before and after etching of the core is shown in Figure 2.

For twenty-nine core/shell NW FETs on which three-probe measurements were conducted, an average n_e of 1.33×10^{19} cm^{-3} and average μ_{FE} of 19.2 $cm^2(V•s)^{-1}$ were found. The same devices, after etching of the GaAs core, exhibited an average n_e of 1.41×10^{19} cm^{-3} and an average μ_{FE} of 32.0 cm^2 $(V•s)^{-1}$. Sample three-probe I_D-V_G curves are shown in Figure 3. For all the parameters, the data showed a large spread most likely related to the device processing.

It was expected that the removal of the GaAs core would allow for the formation of donor-type surface states on the inner surface of the InAs nanotubes in addition to those already present on the outer surface, thus increasing n_e and decreasing ρ. The lack of a significant increase in n_e found experimentally suggests the possible formation of InGaAs at the GaAs/InAs interface. Meanwhile, the small increase in μ_{FE} and decrease in ρ found might still be attributed to relaxation of dislocations associated with the GaAs/InAs interface.

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References:

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[2] Blömers, C., et al. Nanotechnology, 24(3), 035203.

[3] Dayeh, S., et al. Small, 3(2), 326-32.